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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/176,315
Filing Date: October 22, 1998
Appellant(s): MAEDA ET AL.

Raymond F. Cardillo, Jr.
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 18 August 2003.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

Appellant's brief includes a statement that claims 1, 2, 5, and 18 do not stand or fall together and provides reasons as set forth in 37 CFR 1.192(c)(7) and (c)(8).

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

5,767,549	Chen et al.	6-1998
4,899,202	Blake et al.	2-1990

5,023,488	Gunning	6-1991
3,855,610	Masuda et al.	12-1974
JA6-224302	Agari, Hideki	8-1994

Iwamatsu, T., et al., "High-Speed 0.5um SOI 1/8 Frequency Divider with Body-Fixed Structure for Wide Range of Applications," Extended Abstracts of the 1995 International Conference of Solid State Devices and Materials, Osaka, Japan, pp 575-577.

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1-5 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwamatsu et al. in view of Agari and Chen et al., and also in view of Blake et al., Gunning, and Masuda et al.

The first three references are regarded as the primary references. Blake et al., Gunning, and Masuda et al. are relied upon for definitions, and for teachings which would be part of the knowledge of those having ordinary skill in the art.

With respect to claim 1, a method of designing a semiconductor device is claimed. The device includes a MOS transistor on an SOI substrate including a supporting substrate. Iwamatsu et al. shows such a device in Figure 1, where "NMOS," for example, designates MOS transistors. The substrate is "buried oxide" plus "Si-substrate," where SOI is read as "silicon on insulator," with "silicon" being the layer

including the transistor, and "insulator" being the buried oxide. The substrate includes "Si-substrate," which is a supporting substrate. The MOS transistors are operated at a predetermined frequency, where "clock" is understood to mean whatever determines (or "predetermines") the operating frequency of the transistors. This interpretation is consistent with the usage of the term "clock" in the specification, which does not define the term, but uses the term interchangeably with "operating frequency." In the Iwamatsu device, the operating frequency of the transistors is determined by the frequency of the input signal. (The abstract says the "maximum operation frequency is 2.1 GHz.") So the phrase "MOS transistor being operated based on a predetermined clock" is read as describing a MOS transistor being operated at the frequency of the input signal. Alternatively, "clock" could be read on some specific circuit that sets the frequency of the input signal to this frequency divider, not specifically taught in this reference, but inherent, or alternatively obvious, because the frequency of the input signal had to be determined at some point.

The Iwamatsu transistor comprises first and second semiconductor regions of a first conductivity type (N+) formed (or selectively formed) in the SOI layer, as source and drain regions of an NMOS transistor. The regions are formed "independently" because if source and drain are not separated, the device would not function as a transistor. The transistors are formed in a P-type layer which surrounds all of the N+ type source and drain regions. This P-type layer is identified as "a body portion of a second conductivity type," and the portion of the P-type layer which lies between the source and the drain (under the gate as shown in the figure) is identified as a "body

region." A gate electrode is shown above gate oxide, and the body contact is shown in the figure as "Body contact." The body contact is electrically connected to the P-type layer that surrounds all of the source and drain regions, and therefore it is electrically connected to that part of the P-type layer that lies between source and drain regions (the body region). The potential of this contact is fixed (column 1, second full paragraph, "body-fixed SOI").

The claim is drawn to a method, and two method steps are recited. The first step is to provide an operating frequency for the clock. In the Iwamatsu device, as noted above, the input signal can be regarded as the "clock," or the signal that determines the operating frequency of the transistor. The claim limitation is therefore met by providing an operating frequency for the input signal. It would have been obvious to provide an operating frequency for the input signal, because the input signal for a frequency divider has to have a frequency. Alternatively, as noted above, "clock" can be read as the circuit that determines the frequency of the input signal, with the method steps again obvious because the input signal for a frequency divider must have some frequency.

The second method step is to determine a layout pattern of the MOS transistor, such that the RC time constant provided by the gate capacitance and the resistance of the current path between the body region and the body contact is less than 1/500 MHz. Any prior art transistor would have to be designed by a method including a step of determining a layout pattern, because transistors each must have some specific geometry, so the only way to determine whether this claim limitation is infringed would be to decide if the current path is associated with an RC time constant that meets the

given limitation. In other words, this claim limitation is not understood to provide any specific limitations on the geometry of the layout (such as the width of the gate, for example) because any current path that is designed to meet the limitation on the RC time constant would meet the claim limitation.

Iwamatsu et al. does not specifically discuss RC time constants. Chen et al. is a teaching of SOI transistors, similar to Iwamatsu et al. in that the transistors have N+ source and drain regions, and are formed in a P-type layer, or body portion which surrounds the N+ source and drain regions. Figure 1 shows a vertical cross section of the Chen transistors, and figure 3 shows a top view. Figure 3 also shows substrate contact 39 (column 7, lines 25-34), which is analogous to the body contact of Iwamatsu et al. The Chen teaching at column 7, lines 25-34, states that the RC time constant in the body link or recessed region 20 from a respective channel to substrate contact 39 can be as short as or less than 1 nsec. The recessed region 20, in the Chen device, is the continuous sheet of Si which surrounds the N+ source and drain regions, as shown in Chen figure 3. Parts of this continuous p layer extend under the channel regions, as shown in the top view of figure 3. Figure 1 also shows "p-Si" in both the recessed part of the sheet, and in the parts of the sheet that extend under the channel. The Chen teaching at column 7 is to design the device such that the RC time constant for the current path from the body region associated with a respective channel, through the continuous sheet of Si, to body contact 39 is less than 1 nsec. 1 nsec corresponds to an inverse maximum operating frequency of 1/1000 MHz. (1 divided by 10^{9} sec^{-1} is 10^{-9} sec)

Agari teaches in the abstract that it is desirable to minimize RC delay from the resistance value and the capacitance value at each wiring part associated with a layout. It would have been obvious to design the Iwamatsu layout such that the RC time constant associated with the body link is less than 1/1000 MHz, as taught by Chen et al., in order to minimize delay and allow for high frequency operation, as taught by both Chen et al. and Agari. There are two differences between the Chen teaching and the claim limitation of RC less than 1/500MHz. The first is that the frequency is 500 MHz. It would have been obvious to design the body link current path, such that the RC delay is less than 1/500MHz, in order to obtain a device that operates at a frequency at least as high as 500 MHz. Because the Iwamatsu device actually operates up to 2.1 GHz, the RC time constant of its body link would have meet the limitation of RC < 1/500Mz, and an operating frequency of at least 500 Mz, with associated RC time constant, would have been obvious as part of a design method, in order to design a device that would operate at GHz frequencies, like the Iwamatsu device.

The second difference between the Chen teaching related to RC time constant, and the claim limitation, is that the claim limitation applies only to the capacitance contribution to the time constant provided by the gate capacitance. Examiner understands that the Chen teaching applies to the total capacitance that contributes to the RC time constant of the current path within the body link. If the total RC time constant is too large, then the device will not work at the desired frequency. Thus each contribution to the RC time constant must be less than the design value, if the total RC time constant is to be as short as or less than the design value. Thus if a device is

designed according to the Chen teaching, such that the RC time constant of the body link is less than a desired value, then that design process would necessarily give rise to a device having a body link RC time constant contribution from the gate capacitance that is itself less than the desired value. This is all that the claim language requires.

Alternatively, the Gunning reference is relied upon to teach that the discharge of the gate capacitance through the substrate, specifically, is known. See column 7, lines 5-10. Masuda et al. teaches at column 2, lines 40-47, various known capacitances associated with a MOS transistor. In particular, gate-to-substrate capacitance is taught at lines 43-44. And, as noted above, the Agari reference teaches that the total RC time constant for any current path is the result of all contributing RC time constants. In view of these teachings, it would have been obvious to design a transistor having an RC time constant contribution from the gate capacitance to be less than a desired value determined by the frequency of operation, because the current path through the body link is known, the discharge of the gate capacitance through this current path is known, the association of this current path with a total RC time constant is known, the contribution of each known capacitance to the total RC time constant is known, and because the minimization of RC time constant based on desired operating frequency is known.

Claim 2 recites the same limitations as claim 1, except that, instead of operating frequency, the formula is expressed in terms of time itself, instead of frequency. These are two ways of stating the same thing.

Claims 3 and 4 are expressed in product-by-process form, and are drawn to devices made by the design processes of claims 1 and 2. As noted above, the Iwamatsu device operates at a frequency as high as 2.1 GHz. If the contribution to the RC time constant to any current path from any source, known or unknown, is greater than 1/500 MHz, the device could not operate at the stated GHz frequencies, because the signal would discharge through the parasitic or undesired capacitance, instead of passing through the circuit. So the structure produced by the process limitations of claims 1 and 2 would not be distinct from that of the prior art, because the layout of the Iwamatsu device would necessarily meet the limitation on RC time constant set forth in claims 1 and 2. Alternatively, it would have been obvious to produce a structure designed by the processes of claims 1 and 2, because, as noted above, the process steps are themselves known, or obvious variants of known process steps.

Examiner disagrees that claim 3 should stand or fall with claim 1, and that claim 4 should stand or fall with claim 2, as stated by Appellant. Product-by-process claims are drawn to the product produced, and are therefore not analyzed in the same manner as the process itself.

Claims 5 and 18 describe the resistance for a current flow path for the body link in terms of resistivity and geometrical features. This formula appears to describe the resistance of any current flow path, having a resistivity, length, width, and thickness, and extending between a body region of a transistor and a body contact, and would thus describe the prior art current flow path(s) of Iwamatsu. Note again that these two

claims are drawn to structure, in product-by-process form, and in such a claim it is the structure itself that must distinguish. The record does not indicate anywhere any structural difference arising from the limitation(s) of the formula in these claims.

The Blake reference was cited to address the meaning of the term "body." Blake et al. teaches the definition of a transistor "body." See, for example, column 1, lines 55-58 ("the undepleted volume within the body region underlying the gate electrode"). See also reference to the "body region" in column 5, lines 23, 33, 37, and 53-60). So when Chen et al. refers to the "body" of the transistor, one of ordinary skill would know that such a reference includes the region underlying the gate electrode of the transistor. So, with respect to Chen region 20, called the "body link" (column 7, line 32), the examiner understands this to mean that Chen region 20 is what links the Chen transistor body to the body contact 30 (as shown in Chen figure 3).

(11) Response to Argument

Appellant notes that no one reference teaches the method steps of i.e. claims 1 and 2. The rejection is based on the combination of teachings as set forth above, however. Each reference is relied upon for the specific teachings discussed at length above.

Appellant apparently argues that the Chen teaching of doping is not a step of providing an operating frequency. Of course not. The operating frequency is a design parameter. But if one wants a device or circuit to operate at high frequencies, then the

RC time constant of each of the current flow paths must be such that the signal can propagate along the path, rather than be shorted out through a parasitic (or other) capacitance. And, the higher the frequency, the lower the impedance of any capacitance. So the design of a high frequency device or circuit necessarily involves consideration of the resistance and capacitance associated with any and all of the current flow paths.

Part of the problem is in the wording of the claims, which states that a layout *pattern* is to be determined to satisfy a given condition on resistance and capacitance. But resistance and capacitance are determined by a number of factors in addition to the simple geometric pattern of a layout. And any device has some geometric layout. The claim language of i.e. claims 1 and 2 specifically states that the layout meets the required method step, *if the condition on the RC time constant is met.* Method step (b) is infringed if the limitation on RC time constant is met by whatever layout is used. No matter what the layout pattern is, and no matter what the resistivity of the material is. *All the claim limitation provides is a limitation on the RC time constant of the final structure produced.* There is no way to analyze the claim language, whether in view of anticipation/obviousness, or in view of infringement, without considering whether the *structure* produced corresponds to the limitation on RC time constant. (How the limitation on RC time constant is met, whether by modifying the length or width of the current flow path, by adjusting its resistivity, or by modifying the parasitic capacitance itself, is not specified by the claim language.)

And it is salient to note that the structure of Iwamatsu et al. operates at its desired GHz frequency, so the RC constant of the body link must meet the structural limitation set forth in the claim. And, in view of the teachings related to RC time constant in the other references, the fact that the Iwamatsu circuit worked as designed was probably not an accident.

Appellant notes that technical facts of esoteric technology must be supported by citation of some reference work. Apparently, no specific reference teaching in any of the references relied upon by the examiner is disputed. There is absolutely nothing wrong with relying on teachings in patents, rather than "reference works" of some other sort, in order to understand how terms of art are used by those working in the art. Moreover, this is in no way "esoteric technology." The definitions of transistor device regions are covered in the basic course in semiconductor devices in an electrical engineering curriculum, and the problems associated with RC time constant and capacitance are covered in the basic course on circuit theory.

Appellant continues to interpret the "body" of the Chen teaching as being something completely unrelated to the body portion, body region, or body contact of the claims. As discussed at length above, the examiner understands that the Chen body link is that part of the p-type sheet from a respective channel to substrate contact 39. If one only looks at figure 1 of Chen, the association of the body link 20 with only one p-type region in the figure might be confusing. But when one looks at figure 3, it is quite clear that the p-type layer is a continuous sheet that surrounds each transistor, and provides the current flow path between the p-type region under each transistor channel

to the body contact 39. This is not some mysterious usage of the terminology. There is a current flow path from the body region, which is associated with the transistor, all the way over to the contact 39. *The current flows through sheet 20, which must be doped as taught in column 7, in order to minimize its RC time constant.* The region marked 20 in figure 1 is only a small part of the total current flow path. And one must look at figure 3 in order to see that sheet 20 is in electrical (and physical) contact with the regions under the transistor channels. The cross section of figure 1 simply does not show the whole geometry.

Appellant argues that the gate capacitance as set forth in the claims somehow differs from the gate capacitance discussed in the prior art. This interpretation is not consistent with Appellant's specification. Nothing in the specification discusses specifically what Appellant mean by gate capacitance. This term is set forth for example in the sentence spanning pages 18 and 19, which states only that the gate capacitance of the gate electrode having gate length L and gate width W is determined by the capacitance between the gate electrode and the underlying substrate or channel. The formula given is the formula for a parallel plate capacitor, where one plate is the gate electrode and the other plate is the underlying semiconductor. One cannot argue that the claim language means something different from what is taught in the specification. The specification uses gate capacitance in its normal sense, as describing a gate-to-substrate capacitive coupling. This is exactly what Gunning describes, and this parallel plate capacitor is exactly what one of ordinary skill would associate with the term "gate capacitance." The gate capacitance is simply the

capacitor one sees when one looks at a picture of the transistor, with the gate dielectric corresponding to the capacitor dielectric. And, like any parallel plate capacitor, the current that charges and discharges the capacitor plates must flow through the current flow paths on each side of the dielectric. A one-sided capacitor, having only a top gate electrode, with no current flow path associated with the semiconductor layer that provides the lower electrode, would make no sense at all, and the prior art simply does not teach such a one-sided capacitor.

In summary, the design of a high frequency device or circuit to minimize the RC time constant of each of the current flow paths is known. Agari teaches this concept. Gate capacitance is known (Masuda et al.) and the specific current flow path provided by the discharge of the gate capacitor through the underlying substrate is known. Gunning teach this concept. The minimization of RC time constant associated with the this current flow path along the body link in an SOI device is known. Chen et al. teaches this concept. The operating frequency recited in the claims is known. Iwamatsu teaches GHz frequencies. Each of the device or circuit structures set forth in the claims is shown in the references. It would have been obvious to design a semiconductor device to operate at the frequencies taught by Iwamatsu et al., including the design of a body link having a total RC time constant that would allow for device operation at such frequencies, because one wants the device to actually operate at the frequencies it is designed for. And it would have been obvious to include the contribution of the gate capacitance to the total RC time constant of the body link

current flow path, because this capacitance is known, and because all capacitances,

both known and unknown, contribute to the total RC time constant

For the above reasons, it is believed that the rejections should be sustained. As always, the signature of the conferees below does not necessarily indicate agreement with the positions set forth above.

Respectfully submitted,

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January 31, 2005

Conferees

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